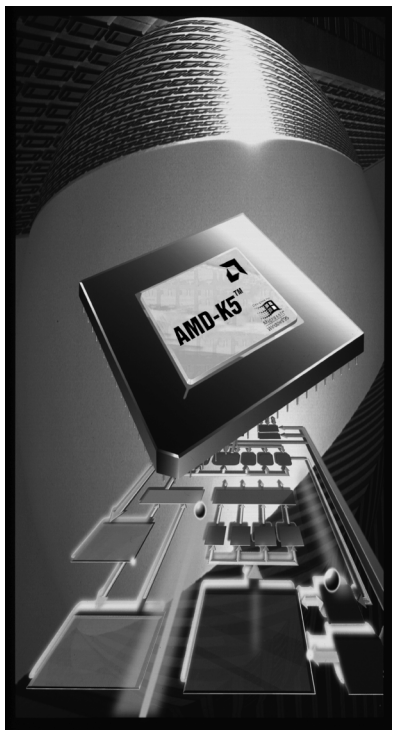
AMD



AMD-K5™

Processor

Data Sheet Amendment

Publication # **18522** Rev: **E** Amendment/**1**
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1 AMD-K5™ Processor Data Sheet Amendment

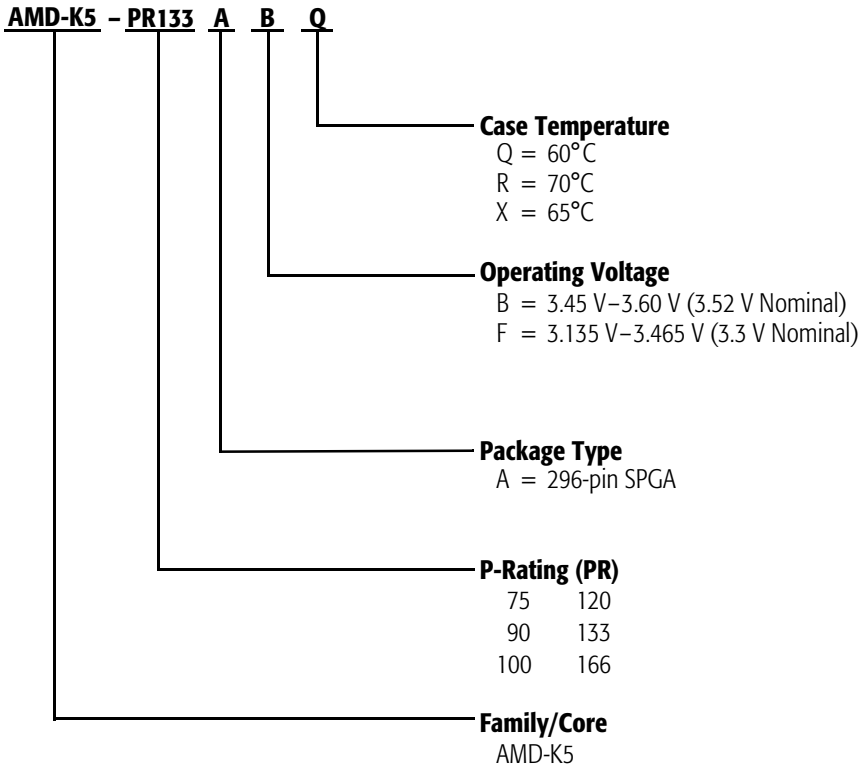
Amendment Contents

- New Ordering Information
  - The PR166 OPN is added
  - The valid combinations are updated
- CPU Identification Updated
  - Manufacturer in JTAG ID code changed to bits 11–1
  - Model 2 added
  - P-Rating information added
- BF1–BF0 Pins Updated
  - 1.75 clock multiplier added
- New Data Cache Write Allocate Information
- DC Characteristics Updated
  - I_{CC} is updated
- Package Thermal Specifications
  - Table 28A for PR75, PR90, and PR100 model 0 processors
  - Table 28B for PR120, PR133, and PR166 model 1 and model 2 processors
- Pipelining
  - Updated specifications for pipelining
  - Timing diagrams

3 Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations

OPN	Package Type	Operating Voltage	Case Temperature
AMD-K5-PR166ABX	296-pin SPGA	3.45 V–3.60 V	65°C
AMD-K5-PR133ABR	296-pin SPGA	3.45 V–3.60 V	70°C
AMD-K5-PR133ABQ	296-pin SPGA	3.45 V–3.60 V	60°C
AMD-K5-PR120ABR	296-pin SPGA	3.45 V–3.60 V	70°C
AMD-K5-PR100ABQ	296-pin SPGA	3.45 V–3.60 V	60°C
AMD-K5-PR90ABQ	296-pin SPGA	3.45 V–3.60 V	60°C
AMD-K5-PR75ABR	296-pin SPGA	3.45 V–3.60 V	70°C

Notes:

1. *Valid combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.*

5 CPU Identification

Upon completion of RESET, the DX register contains a component identification. The upper byte of DX (DH) will contain 05h. The lower byte of DX (DL) will contain a CPU model (0h–2h)/stepping identifier (xh).

CPU ID						
Family ID (DH)	**Model ID (DL, top 4 bits)**	**CPU Frequency (MHz)**	**Bus Speed**	**Processor P-Rating**	**BF Pin**	**BF1–BF0 Pins**
5	0	75	50	AMD-K5-PR75	1	N/A
		90	60	AMD-K5-PR90	1	N/A
		100	66	AMD-K5-PR100	1	N/A
	1	90	60	AMD-K5-PR120	N/A	10
		100	66	AMD-K5-PR133	N/A	10
	2	116.7	66	AMD-K5-PR166	N/A	00

Notes:
This table does not constitute product announcements. Instead, the information in the table represents possible product offerings. AMD will announce actual products based on availability and market demand

The boundary scan test access port (TAP) returns the following information in the device identification register (DIR).

JTAG ID Code					
Version (Bits 31–28)	**Bond Option (Bit 27)**	**Unused (Bits 26–24)**	**Part Number (Bits 23–12)**	**Manufacturer (Bits 11–1)**	**LSB (Bit 0)**
xh	xb	000b	50xh (Model 0) 51xh (Model 1) 52xh (Model 2)	00000000001b	1b

Note: *The following information updates the BF1–BF0 pins on page 15 of the data sheet.*

BF1–BF0 (Model 1 and Model 2)

Bus Frequency Input

For the AMD-K5 model 1 and model 2 processors, the BF1 and BF0 signals determine the internal operating speed of the processor. The frequency of the CLK signal is multiplied internally by a ratio determined by the states of the BF1 and BF0 signals during RESET. The processor speed multiplier is determined as shown below:

BF1 Pin	BF0 Pin	Internal Clock Multiplier
0	0	1.75
0	1	Reserved
1	0	1.5
1	1	1.5

Note: *The following information concerning write cycles and write allocate logic updates the information on pages 33 and 34 of the data sheet.*

Write Cycles

Processor writes that hit in modified or exclusive lines in the data cache require no external data cycle. The data is updated in the cache. Processor writes that hit shared lines of the data cache update the data cache and memory. The status returned with the writethrough bus cycle determines the final state of the line.

If write allocate is enabled in the AMD-K5 processor, processor writes that miss in the data cache generate an external data cache read cycle followed by a write hit. If write allocate is not enabled in the AMD-K5 processor, write misses generate an external write cycle only.

Write Allocate

Write allocate is an operating mode of the AMD-K5 processor that causes cache write misses to either proceed as normal write misses or to be converted to data cache line fills followed by cache write hits. The write allocate feature provides improved performance on repeat accesses to write-allocated data cache lines. The load/store unit in the processor determines whether each cache write miss is write-allocatable by whether it falls in or out of the ranges specified in the memory range registers.

For details on the implementation of write allocate, refer to the *AMD-K5 Processor Software Development Guide*, order# 20007.

Before the write cycle occurs for a write miss with write allocate enabled, an external data cache read cycle occurs that follows the normal rules for read allocate, and the intermediate state of the filled data cache line depends on the result of the read cycle as shown in Table 8. The final state of the data cache line is determined as shown in Table 9 by the transition from the intermediate read state (M, E, S, or I) to the final state (M, E, S, or I) after the write hit to the cache line.

Note: *In write allocate mode, replaced data cache lines are handled in the same way as during read allocate.*

Table 9. Writes to Data Cache

State	$\overline{\text{CACHE}}$	$\overline{\text{KEN}}$	WB/$\overline{\text{WT}}$	PWT	Next State	Note
M	x	x	x	x	M	1
E	x	x	x	x	M	2
S	0	0	1	0	E	3
S	0	0	0	x	S	3
	0	0	x	1		
I	x	x	x	x	I	4

Notes:

1. *A write hit to modified line: writes data to the cache.*
2. *A write hit to exclusive line: writes data to the cache.*
3. *A write hit to shared line: writes data to the cache and memory; invalidates any shared copy in the other cache.*
4. *If write allocate mode is not enabled, an invalid line always remains invalid. If write allocate mode is enabled, the intermediate state of the filled data cache line depends on the result of the read cycle as shown in Table 8, and the final state of the data cache line is determined by the intermediate state as applied to this table.*

9.3 Operating Ranges

See "Ordering Information" on page 2 for the standard products that are available for the AMD-K5 processor.

Commercial (C) Devices

T_{CASE} ..... 0°C to +70°C
V_{CC} ..... 3.3 V ± 5%

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

Table 14. DC Characteristics over Commercial Operating Ranges

Symbol	Parameter Description	Advance Info		Comments
		Min	Max	
V_{IL}	Input Low Voltage	–0.3 V	+0.8 V	
V_{IH}	Input High Voltage	2.0 V	V_{CC}+0.3 V	
V_{OL}	Output Low Voltage		0.4 V	I_{OL} = 4-mA load
V_{OH}	Output High Voltage	2.4 V		I_{OH} = 1-mA load
I_{CC}	Power Supply Current—Model 0		44.0 mA/MHz	V_{CC} = 3.6 V Note 1
	Power Supply Current—Models 1 and 2		39.0 mA/MHz	V_{CC} = 3.6 V Note 6
I_{LI}	Input Leakage Current		±15 µA	Note 2
I_{LO}	Output Leakage Current		±15 µA	Note 2
I_{IL}	Input Leakage Current Bias with Pull-up (Low)		400 µA	Note 3
I_{IH}	Input Leakage Current Bias with Pull-up (High)		200 µA	Note 4
C_{IN}	Input Capacitance		15 pF	Note 5
C_{OUT}	Output Capacitance		20 pF	Note 5
C_{OUT}	I/O Capacitance		25 pF	Note 5
C_{CLK}	CLK Capacitance		15 pF	Note 5
C_{TIN}	Test Input Capacitance		15 pF	Note 5
C_{TOUT}	Test Output Capacitance		20 pF	Note 5
C_{TCK}	TCK Capacitance		15 pF	Note 5

Notes:

1. *Typical supply current for model 0: 36 mA/MHz (2700 mA at PR75, 3240 mA at PR90, and 3600 mA at PR100).*
2. *This parameter is for inputs or I/O without an internal pull-up resistor and $0 \le V_{IN} \le V_{CC}$.*
3. *This parameter is for inputs with pull-ups and V_{IL} = 0.40 V.*
4. *This parameter is for inputs with pull-downs and V_{IH} = 2.4 V.*
5. *This parameter is determined by design.*
6. *Typical supply current for models 1 and 2: 30 mA/MHz (2700 mA at PR120, 3000 mA at PR133, and 3501 mA at PR166).*

12 Package Thermal Specifications

The AMD-K5 processor is specified for operation when T_{CASE} (the case temperature) is within the range of 0°C to 70°C. T_{CASE} can be measured in any environment to determine whether the AMD-K5 processor is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature (T_A) is guaranteed as long as T_{CASE} is not violated. The ambient temperature can be calculated from θ_{CA} and from the following equation:

$$T_{CASE} = T_A + (P \bullet \theta_{CA})$$

where:

T_A, T_{CASE} = Ambient and Case Temperature
θ_{CA} = Case-to-ambient Thermal Resistance
P = Maximum Power Consumption

The value for θ_{CA} is given in Table 27 for the 1.90 sq. in., 296-pin, ceramic SPGA case. Maximum T_A is shown in Table 28. The values for processor frequency in Table 28 apply to the AMD-K5 processors model 0, model 1, and model 2.

Table 27. θ_{CA} for the AMD-K5 Processor in 296-pin SPGA Package for Typical Heat Sinks with Fans

Heat Sink With Fan (length x width x height)	θ_{CA} (°C/W)	Manufacturer - Part Number
1.885 in x 1.9 in x 1.04 in	0.81	Thermalloy, Inc. - 20961-TCM
1.95 in x 1.79 in x 1.06 in	1.3	Wakefield Engineering, Inc. - 709-100AB124
1.96 in x 1.96 in x 0.65 in	1.5	AAVID - 355455F00267

Notes:
1. *Thermal interface material (e.g., thermal grease or thermal compound) is required between the top of the processor case and the base of the heat sink.*

Table 28A. Model 0 Maximum T_A in °C

Heat Sink	Airflow of 0 (0) ft/min. (m/sec)		
	PR75[1]	PR90[2]	PR100[3]
Thermalloy Heat Sink w/Fan	60.6	48.7	47.5
Wakefield Heat Sink w/Fan	54.9	41.9	39.9
AAVID Heat Sink w/Fan	52.6	39.1	36.8

Notes:

1. $T_{CASE} = 70°C$, $V_{CC} = 3.52$ V, $I_{CC} = 3300$ mA
2. $T_{CASE} = 60°C$, $V_{CC} = 3.52$ V, $I_{CC} = 3960$ mA
3. $T_{CASE} = 60°C$, $V_{CC} = 3.52$ V, $I_{CC} = 4400$ mA

Table 28B. Models 1 and 2 Maximum T_A in °C

Heat Sink	Airflow of 0 (0) ft/min. (m/sec)		
	PR120[1]	PR133[2]	PR166[3]
Thermalloy Heat Sink w/Fan	60.0	48.9	52.0
Wakefield Heat Sink w/Fan	53.9	42.2	44.2
AAVID Heat Sink w/Fan	51.5	39.4	41.0

Notes:

1. $T_{CASE} = 70°C$, $V_{CC} = 3.52$ V, $I_{CC} = 3510$ mA
2. $T_{CASE} = 60°C$, $V_{CC} = 3.52$ V, $I_{CC} = 3900$ mA
3. $T_{CASE} = 65°C$, $V_{CC} = 3.52$ V, $I_{CC} = 4551$ mA

Pipelining

The following pipeline cycles are supported by AMD-K5 processors model 1 and model 2 with stepping level of 4 and above:

- Cacheable instruction cache cycle into a cacheable instruction cache cycle
- Cacheable instruction cache cycle into a cacheable data cache cycle
- Cacheable instruction cache cycle into a non-cacheable data cache cycle (could be I/O)
- Cacheable instruction cache cycle into a non-cacheable instruction cache cycle
- Non-cacheable instruction cache cycle into a cacheable data cache cycle
- Non-cacheable instruction cache cycle into a non-cacheable data cache cycle
- Cacheable data cache cycle into a cacheable instruction cache cycle
- Cacheable data cache cycle into a non-cacheable instruction cache cycle
- Non-cacheable data cache cycle into a cacheable instruction cache cycle
- Non-cacheable data cache cycle into a non-cacheable instruction cache cycle
- Write cycle (could be I/O) into a write cycle (could be I/O)
- Write cycle (could be I/O) into a cacheable instruction cache cycle
- Write cycle (could be I/O) into a non-cacheable instruction cache cycle
- Write cycle (could be I/O) into a cacheable data cache cycle
- Write cycle (could be I/O) into a non-cacheable data cache cycle

Pipelining is not supported for the following cycles:

- Non-cacheable instruction cache cycle into a non-cacheable instruction cache cycle
- Non-cacheable instruction cache cycle into a write cycle (could be I/O)
- Cacheable instruction cache cycle into a write cycle (could be I/O)
- Non-cacheable data cache cycle into a write cycle (could be I/O)
- Cacheable data cache cycle into a write cycle (could be I/O)
- Cacheable data cache cycle into a cacheable data cache cycle
- Cacheable data cache cycle into a non-cacheable data cache cycle
- Non-cacheable data cache cycle into a non-cacheable data cache cycle
- Non-cacheable data cache cycle into a cacheable data cache cycle

Timing Diagrams

The timing diagrams in Figure 1 and Figure 2 illustrate pipelining.

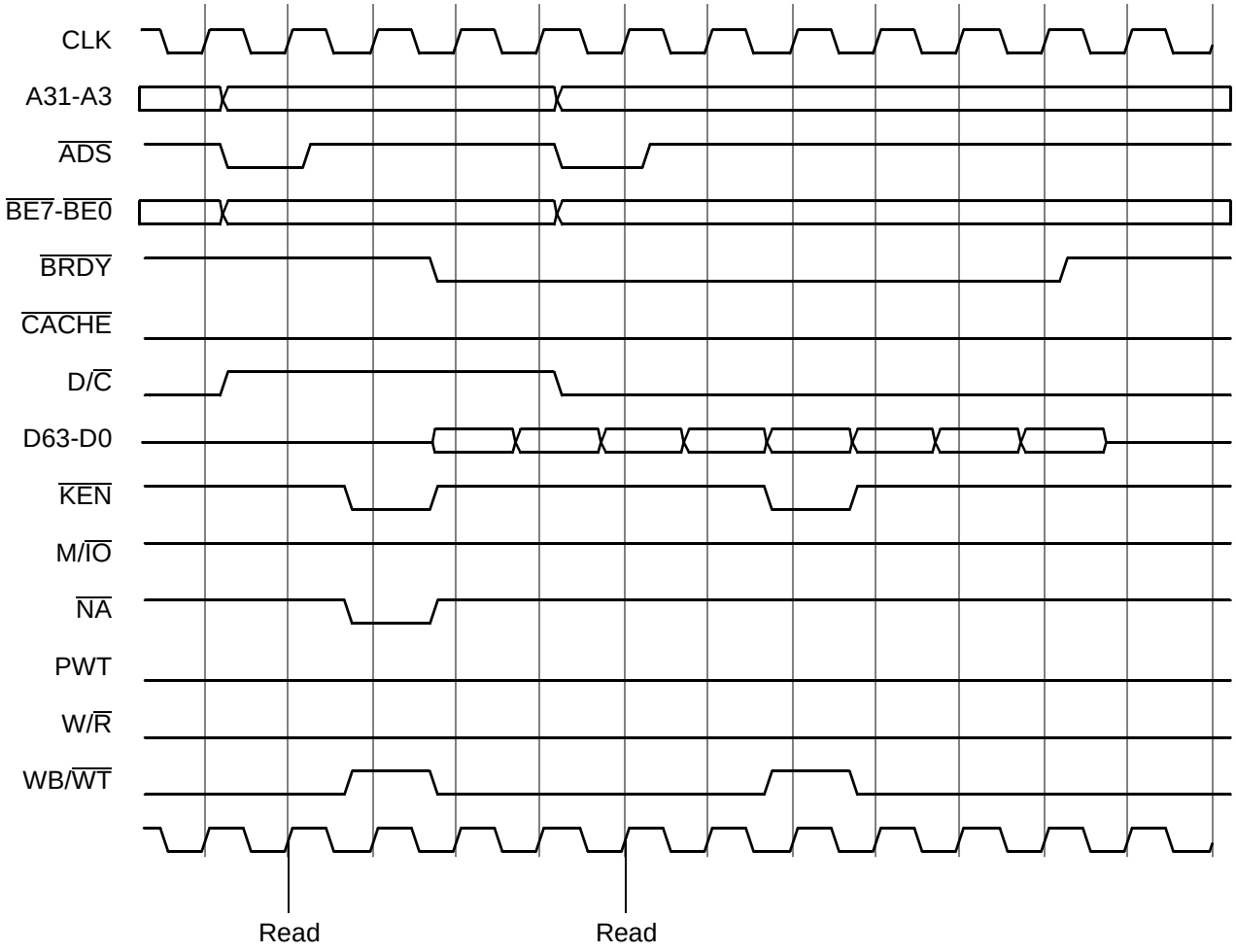


Figure 1. Pipelined Cacheable Data Cache Cycle into a Cacheable Instruction Cache Cycle

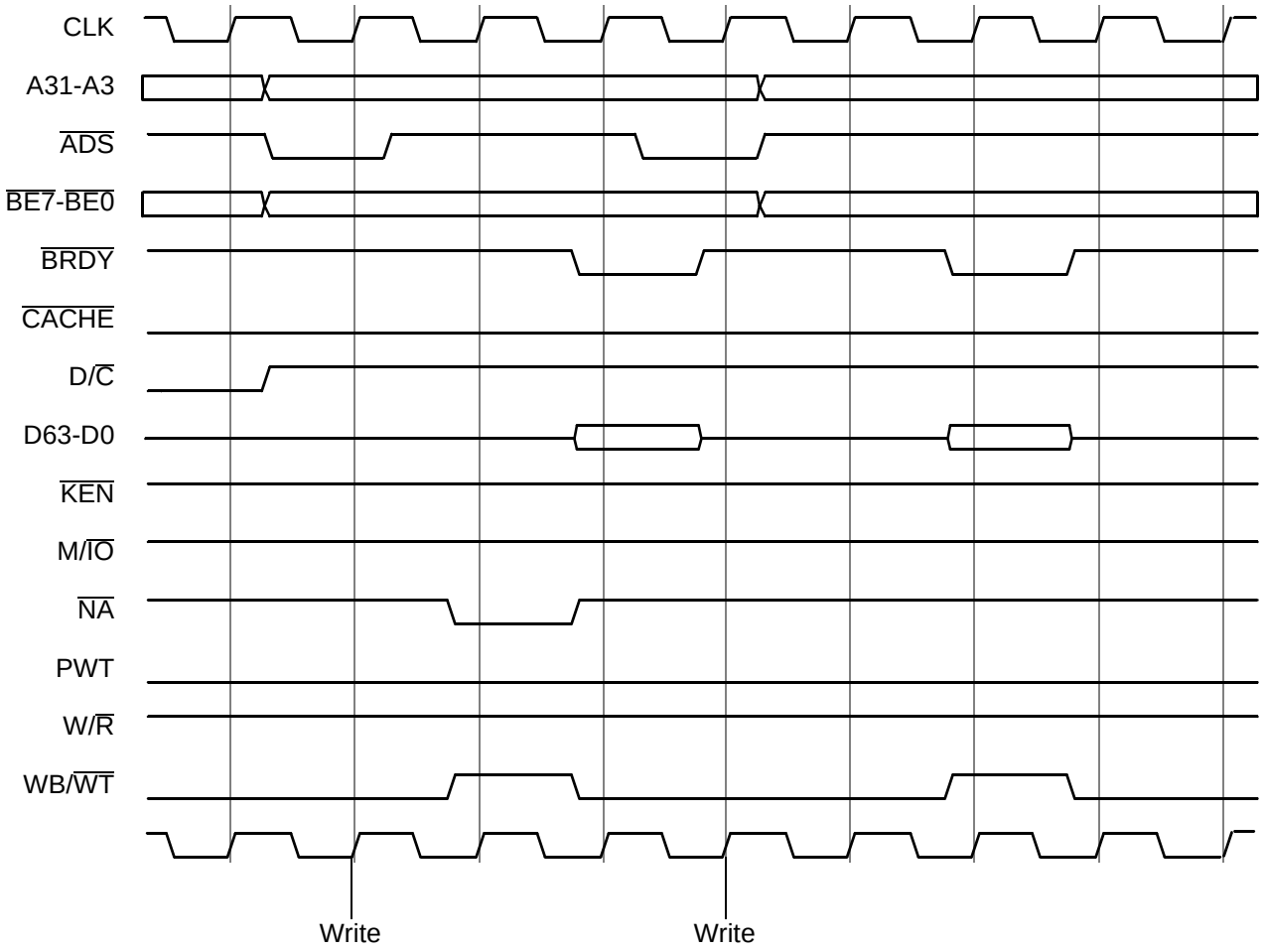


Figure 2. Pipelined Write Cycle (Could be I/O) into a Write Cycle (Could be I/O)

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